IN THE CLAIMS

Please amend the claims as follows:

1. (Cancelled)

2. (Currently Amended) The memory cell of claim [[1]] 74, wherein the selective epitaxy mesa includes a bottom source/drain and a top source/drain, and wherein the selective epitaxy mesa further includes a conductive body separating the bottom source/drain from the top source/drain.

3. (Original) The memory cell of claim 2, wherein the bottom source/drain is an in situ doped region.

4. (Original) The memory cell of claim 2, wherein the top source/drain is an in situ doped region.

5. (Withdrawn) The memory cell of claim 2, wherein the bottom source/drain includes a semi-annular ring around a bottom portion of the selective epitaxy mesa.

6. (Withdrawn) The memory cell of claim 5, wherein the vertical access device includes a signal line having a first height, and wherein the bottom source/drain includes a second height that is about equal to the first height.

7. (Withdrawn) The memory cell of claim 5, wherein the bottom source/drain is formed by out diffusion from an adjacent conductor.

8. (Currently Amended) The memory cell of claim [[1]] 74, wherein the access device is free from a shallow trench isolation layer.

9. (Cancelled)

10. (Currently Amended) The memory cell of claim [[9]] 75, wherein the substrate includes silicon, and wherein the selective epitaxy mesa includes silicon.

11. (Currently Amended) The memory cell of claim [[9]] 75, wherein the access device includes a body, a first source/drain region, a gate and a second source/drain region, wherein the body extends between the first source/drain region and the second source/drain region, and wherein the first source/drain region and the second source/drain region are each a selective epitaxy doped region of the selective epitaxy mesa.

12. (Original) The memory cell of claim 11, wherein the first source/drain region extends horizontally around the selective epitaxy mesa.

13. (Original) The memory cell of claim 12, wherein the first source/drain region is adapted to contact a bit line.

14. (Original) The memory cell of claim 12, wherein the second source/drain region is spaced from the substrate by the body.

15. (Original) The memory cell of claim 14, wherein the second source/drain region is an in situ N+ doped region of the selective epitaxy mesa.

16. (Previously Presented) A vertical memory cell, comprising:

a substrate;

an electrical signal line on the substrate;

an access device including:

a selective epitaxy mesa formed on and extending outwardly from the substrate, the selective epitaxy mesa including a first source/drain region adjacent the substrate and in electrical communication with the electrical signal line, wherein the first source/drain region

includes a lateral non-graded dopant profile consisting essentially of dopant atoms of one conductivity type; and

a storage device on the selective epitaxy mesa.

17. (Original) The vertical memory cell of claim 16, wherein the electrical signal line has a first height, and wherein the first source/drain region has a second height equal to or less than the first height.

18. (Original) The vertical memory cell of claim 16, wherein the selective epitaxy mesa cantilevers upwardly from the substrate, and wherein the selective epitaxy mesa includes an end, remote from the substrate, forming a second source/drain region.

19. (Original) The vertical memory cell of claim 16, wherein the first source/drain region extends around an outer periphery of the selective epitaxy mesa.

20. (Original) The vertical memory cell of claim 19, wherein the electrical signal line extends around the first source/drain region.

21. (Withdrawn) The vertical memory cell of claim 16, wherein the first source/drain region extends partially around an outer periphery of the selective epitaxy mesa.

22. (Withdrawn) The vertical memory cell of claim 21, wherein the electrical signal line extends around the first source/drain region.

23. (Withdrawn) The vertical memory cell of claim 21, wherein the electrical signal line partially around the selective epitaxy mesa.

24. (Original) The vertical memory cell of claim 16, wherein the first source/drain region is adapted to electrically communicate with a column address decoder through a buried bit line.

25. (Original) The vertical memory cell of claim 24, wherein the second source/drain region is adapted to electrically communicate with the storage device.

26. (Previously Presented) A vertical memory cell, comprising:

a substrate;

an electrical signal line on the substrate;

an access device including a selective epitaxy mesa formed on and extending outwardly from the substrate, the selective epitaxy mesa including a first source/drain region adjacent the substrate and in electrical communication with the electrical signal line, the first source/drain region of the selective epitaxy mesa includes a laterally non-graded dopant profile consisting essentially of dopant of one conductivity type, the selective epitaxy mesa further including a body extending vertically from the first source/drain region, an insulator on the body, and a gate on the insulator; and

a storage device on the selective epitaxy mesa remote from the substrate.

27. (Original) The vertical memory cell of claim 26, wherein the insulator surrounds the body, and wherein the gate surrounds the insulator such that the gate effects electrical conductivity of the body from more than one angle.

28. (Withdrawn) The vertical memory cell of claim 26, wherein the insulator surrounds the body, and wherein the gate partially overlies the insulator such that the gate effects electrical conductivity of the body from more than one angle.

29. (Withdrawn) The vertical memory cell of claim 28, wherein the gate overlies over half of a surface area of the body.

30. (Original) The vertical memory cell of claim 26, wherein the electrical signal line includes titanium.

31. (Cancelled)

32. (Currently Amended) The transistor of claim [[31]] 76, wherein the body is adapted to form a channel between the doped first region and the doped second region.

33. (Currently Amended) The transistor of claim [[31]] 76, wherein the first doped region is adapted to be in electrical ~~electrically~~ communication with the buried bit line.

34. (Currently Amended) The transistor of claim [[31]] 76, wherein the gate is adapted to be in electrical communication with a word line.

35. (Currently Amended) The transistor of claim [[31]] 76, wherein the gate overlies at least half of the surface area of the intermediate region.

36. (Currently Amended) The transistor of claim [[31]] 76, wherein the gate overlies at least about 75% of the surface area of the intermediate region.

37. (Currently Amended) The transistor of claim [[31]] 76, wherein the gate overlies about all of the surface area of the intermediate region.

38. (Currently Amended) The transistor of claim [[31]] 76, wherein the vertical, selective epitaxy body is generally cylindrical.

39. (Original) The transistor of claim 38, wherein the gate is generally annular and extends completely around the body.

40. (Original) The transistor of claim 38, wherein the first doped region is cylindrical.

41-70. (Canceled)

71. (Currently Amended) The memory cell of claim [[1]] 74, wherein the selective epitaxy mesa includes a region of polycrystalline silicon.

72. (Currently Amended) The memory cell of claim [[1]] 74, wherein the region of the selective epitaxy mesa adjacent to the buried conductive path comprises at least one abrupt p-n junction.

73. (Currently Amended) The memory cell of claim [[1]] 74, wherein the region of the selective epitaxy mesa adjacent to the buried conductive path comprises at least one abruptly doped region.

74. (New) A memory cell, comprising:

a vertical access device including a selective epitaxy mesa, wherein the selective epitaxy mesa comprises a portion of a buried conductive path, and wherein a region of the selective epitaxy mesa adjacent to the buried conductive path includes a laterally non-graded dopant profile consisting essentially of dopant of one conductivity type; and

a storage device on the selective epitaxy mesa.

75. (New) A vertical memory cell, comprising:

a substrate;

an access device including a selective epitaxy mesa formed on and extending outwardly from the substrate, wherein the selective epitaxy mesa comprises a portion of a buried conductive path, and wherein a region of the selective epitaxy mesa adjacent to the buried conductive path includes a laterally non-graded dopant profile consisting essentially of dopant of one conductivity type; and

a storage device on the selective epitaxy mesa.

76. (New) A vertical transistor, comprising:

a vertical, selective epitaxy body extending from a horizontal substrate such that a portion of the selective epitaxy body is adapted to comprise a vertical portion of a buried bit line, wherein a region of the selective epitaxy body adjacent to the vertical portion includes a laterally diffused dopant concentration profile consisting essentially of dopant of one conductivity type;

a first doped region in the body adjacent the substrate;

an undoped intermediate region between the first doped region and the second doped region; and

a gate at least partially surrounding the intermediate region.

77. (New) A vertical memory cell, comprising:

a substantially planar surface;

an access device including a mesa, the mesa formed partly within an annular depression and extending outwardly from the planar surface;

a first and a second insulator forming a portion of the annular depression;

a buried conductive path bounded by the first and a second insulator, the buried conductive path enclosing a section of the mesa, the mesa circumferentially contacting the buried conductive path at a specified radius above the first insulator, wherein a portion of the mesa extending radially inward from the buried conductive path and extending vertically along the buried conductive path between the first insulator and the second insulator consists essentially of dopant atoms of one conductivity type, and wherein the dopant atoms in the portion form with a diffused concentration profile in the radial direction; and

a storage device on the mesa.

78. (New) The memory cell of claim 77, wherein the first and the second insulators are configured to permit current in the buried conductive path to flow into the mesa only across the specified radius.

79. (New) The memory cell of claim 77, wherein the annular depression is formed with a uniform radius.

80. (New) The memory cell of claim 77, wherein the annular depression is formed having the specified radius.

81. (New) The memory cell of claim 77, wherein the buried conductive path contacts the mesa along the circumference only between the first and the second insulators.

82. (New) The memory cell of claim 77, wherein the buried conductive path is a bit line conductor.

83. (New) The memory cell of claim 77, wherein the mesa electrically contacts the buried conductive path only at the specified radius.

84. (New) The memory cell of claim 77, wherein the mesa includes a diffused dopant concentration profile in a vertical region configured to contact the storage device.

85. (New) A vertical memory cell, comprising:

a substantially planar surface;

an access device including a mesa, the mesa formed partly within an annular recess and extending outwardly from the planar surface;

a first and a second insulator used to form a portion of the annular recess;

a buried conductive path confined by the first and the second insulator, the buried conductive path enclosing a section of the mesa, the mesa circumferentially contacting the buried conductive path at a specified radius above the first insulator, wherein a portion of the mesa extending radially inward from the buried conductive path and extending vertically along the buried conductive path between the first insulator and the second insulator consists essentially of dopant atoms of one conductivity type, and wherein the dopant atoms in the portion arrange in an abrupt concentration profile in the radial direction; and

a storage device on the mesa.

86. (New) The memory cell of claim 85, wherein the first and the second insulators are configured to permit a voltage transmitted along in the buried conductive path to couple to the mesa only at the specified radius.

87. (New) The memory cell of claim 85, wherein the annular recess is formed with a specified radius.

88. (New) The memory cell of claim 85, wherein the annular recess is formed having the specified radius.

89. (New) The memory cell of claim 85, wherein the buried conductive path contacts the mesa only along the circumference between the first and the second insulators.

90. (New) The memory cell of claim 85, wherein the buried conductive path is a bit line conductor.

91. (New) The memory cell of claim 85, wherein the mesa is configured to electrically contact the buried conductive path only at the specified radius.

92. (New) The memory cell of claim 85, wherein the mesa is electrically coupled to a two-part gate conductor.

93. (New) The memory cell of claim 92, wherein the two part gate conductor includes a first conductor and a second conductor, the first conductor having a thickness substantially less than a thickness of a second conductor.

94. (New) The memory cell of claim 93, wherein the first conductor is formed substantially outwardly from the surface around the mesa and the second conductor is formed substantially parallel to the planar surface.

95. (New) The memory cell of claim 93, wherein the first conductor is formed of a polysilicon and the second conductor is formed of a metal.

96. (New) A vertical memory cell, comprising:

a substantially planar surface;

an access device including a mesa, the mesa formed partly within an cylindrical recess and extending outwardly from the planar surface;

a first and a second insulator defining the cylindrical recess at the perimeter;

a buried conductive path bordered by the first and a second insulator, the buried conductive path semi-circularly surrounding the mesa, the mesa contacting the buried conductive path at a specified radius above the first insulator, wherein a portion of the mesa extending radially inward from the buried conductive path and extending vertically along the buried conductive path between the first insulator and the second insulator consists essentially of dopant atoms of one conductivity type, and wherein the dopant atoms in the portion arrange with a specified concentration profile in the radial direction; and

a storage device on the mesa.

97. (New) The memory cell of claim 96, wherein the mesa is configured to receive a voltage signal propagating along the buried conductive path only across the specified radius between the first and the second insulators.

98. (New) The memory cell of claim 96, wherein the cylindrical recess is formed having a uniform radius.

99. (New) The memory cell of claim 96, wherein the cylindrical recess is formed having the specified radius.

100. (New) The memory cell of claim 96, wherein the mesa only contacts the buried conductive path along a perimeter of the mesa.

101. (New) The memory cell of claim 96, wherein the buried conductive path forms a bit line conductor.

102. (New) The memory cell of claim 101, wherein the bit line conductor is formed of polysilicon.

103. (New) The memory cell of claim 96, wherein the mesa contacts the buried conductive path only along the specified radius.

104. (New) The memory cell of claim 96, wherein the mesa includes a horizontal diffused dopant concentration profile in a region in contact with the storage device.

105. (New) The memory cell of claim 96, wherein the buried conductive path is configured to increase a device pitch.

106. (New) The memory cell of claim 96, wherein the buried conductive path is configured as a word line.

107. (New) The memory cell of claim 96, wherein the buried conductive path is located a distance at or above a surface of the mesa nearest the planar surface.

108. (New) The memory cell of claim 96, wherein the specified concentration profile is a diffusion concentration profile.

109. (New) The memory cell of claim 96, wherein the specified concentration profile is an abrupt concentration profile.

110. (New) The memory cell of claim 96, wherein the mesa includes a diffused dopant concentration profile in a vertical region configured to contact the storage device.